**Cell Broadband Engine (BE) Processor**

**OUTLINE**
- Cell History & Highlights
- Challenges in Architectures
- Cell BE Architecture
  - Power Processor Element (PPE)
  - Synergistic Processor Element (SPE)
  - Element Interconnect Bus (EIB)
  - I/O and Memory Interfaces
- Performance Comparison
- Summary & Conclusion

**CELL**
- SCEI/Sony, Toshiba, IBM (STI) Alliance formed in 2000
- Design Center opened in March 2001
- Based in Austin, Texas
- February 7, 2005: First technical disclosures
- May 16, 2005: First public demonstrations at E3
- August 25, 2005: Release of technical documentation

**CELL HISTORY & HIGHLIGHTS**
- Supercomputer on a chip
- Multi-core microprocessor (9 cores)
  - 1 Power Processor Element (PPE)
  - 8 Synergistic Processor Elements (SPEs)
- 3 to 4+ GHz clock frequency
  - Theoretical computing capability of 256 GFLOPS (Giga-Billion Floating Point Operations per Second) at 4GHz
  - 256 GOPS (Integer at 4 GHz)
  - 25 GFLOPS (Double precision at 4 GHz)
- Memory bandwidth of 25.6 GBytes per second.
- I/O bandwidth of 76.8 GBytes per second.

**CELL HISTORY & HIGHLIGHTS (C)**
- 235 mm²
- 235 million transistors.
- 10x performance for many applications
- Cell BE Processor can support many systems
  - Game console systems, HD TV, Servers, Supercomputers etc.
The technology in the Cell is similar to that in GPUs (Graphical Processor Units) so such high performance is certainly well within the realm of possibilities. The big difference is though that Cell is a lot more general purpose so can be usable for a wider variety of tasks. For example, the Nvidia GeForce 6800 Ultra has been observed to reach 40 GFlops in fragment processing. In comparison, the theoretical peak performance of the Intel 3GHz Pentium4 is only 6GFlops.

Such a simple CPU needs the compiler to do a lot of the scheduling work that hardware usually does so a good compiler will be essential. That said, the Cell’s high bandwidth memory and I/O subsystems and the PPE’s high clock speed and dual threading capability may well make up for these potential performance deficiencies.

Cell is an accelerator extension to Power
- Built on a Power ecosystem
- Used best known system practices for processor design
- Sets a new performance standard
- Exploits parallelism while achieving high frequency
- Supercomputer attributes with extreme floating point capabilities
- Sustains high memory bandwidth with smart DMA controllers
- Designed for flexibility
  - Wide variety of application domains
  - Highly abstracted to highly exploitable programming models
  - Virtual trusted computing environment for security

3-WALLS in HIGH PERFORMANCE COMPUTING
- Power Wall
  - Must improve efficiency and performance equally
- Memory Wall
  - Latency induced performance and bandwidth limitations
- Frequency Wall
  - Diminishing returns from deeper and/or wider pipelines

CELL CONCEPT,
- Compatibility with 64b Power Architecture™
  - Builds on and leverages IBM investment and community
- Increased efficiency and performance
  - Attacks on the “Power Wall”
    - Non Homogeneous Coherent Multi-processor
    - High design frequency @ a low operating voltage with advanced power management
  - Attacks on the “Memory Wall”
    - Streaming DMA architecture
    - 3-level Memory Model: Main Storage, Local Storage, Register Files
CHALLENGES IN ARCHITECTURES (C)

<table>
<thead>
<tr>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>12</td>
</tr>
<tr>
<td>13</td>
</tr>
</tbody>
</table>

(continues)

- Attacks on the “Frequency Wall”
  - Highly optimized implementation
  - Large shared register files and software controlled branching to allow deeper pipelines
- Multi-OS support
  - Combine real-time and non-real-time worlds

CELL BE ARCHITECTURE

<table>
<thead>
<tr>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>14</td>
</tr>
<tr>
<td>15</td>
</tr>
</tbody>
</table>

The Cell architecture is like nothing we have ever seen in commodity microprocessors, it is closer in design to multiprocessor vector supercomputers.

All systems are limited by their slowest components [Amdahl’s law], Cell was designed not to have any slow components!

CELL BE ARCHITECTURE (C)

<table>
<thead>
<tr>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>16</td>
</tr>
<tr>
<td>17</td>
</tr>
</tbody>
</table>

- While they can go higher, because of the vagaries of manufacturing, economics and heat dissipation the Cell which will be used in the PS3 is clocked at 3.2 GHz and will have only 7 SPEs. Cells with 6 SPEs will be used in consumer electronics.

CELL BE ARCHITECTURE (C)

<table>
<thead>
<tr>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>18</td>
</tr>
</tbody>
</table>

- Cell is not a collection of different processors, but a synergistic whole
  - Operation paradigms, data formats and semantics consistent
  - Share address translation and memory protection model
- PPE for operating systems and program control
- SPE optimized for efficient data processing
  - Synergistic Processor Unit (SPU)
  - Synergistic Memory Flow Control (MFC)
    - Data movement and synchronization
    - Interface to high-performance Element Interconnect Bus

CELL BE ARCHITECTURE (C)

<table>
<thead>
<tr>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>19</td>
</tr>
</tbody>
</table>

- EIB integrates system as data transport hub
- Main changes compared to x86 architecture
  - RISC design
  - In-Order CPU (instead of Out-of-Order)
  - Heterogeneous Multiprocessing (9-Core Processors)
Vector/SIMD (single instruction stream, multiple data stream) multimedia extension (VMX) technology provides a software model that accelerates the performance of various software applications and runs on reduced instruction set computing (RISC) microprocessors.
- Instruction fetch and decode fetches and decodes four instructions in parallel from the first-level instruction cache for two simultaneously executing threads in alternating cycles.
- When both threads are active, two instructions from one of the threads are issued in program order in alternate cycles. The core contains one instance of each of the major execution units (branch, fixed-point, load/store, floating-point (FPU), and vector-media (VMX). Processing latencies are indicated in part (b).

SYNERGISTIC PROCESSOR ELEMENT
- a.k.a. Streaming Processor Element
- Provides the computational performance
- Simple RISC User Mode Architecture
  - Dual issue VMX-like
  - Graphics SP (Single Precision)-Float (32 bits)
  - IEEE DP (Double Precision)-Float (64 bits)
- Dedicated resources: unified 128x128-bit RF, 256KB Local Store (not cache)
- Dedicated DMA engine: Up to 16 outstanding requests (from LS to Main Memory 1KB to 16KB)

A big difference in Cells from normal CPUs is the ability of the SPEs in a Cell to be chained together to act as a stream processor [Stream]. A stream processor takes data and processes it in a series of steps.
- In order to do stream processing an SPE reads data from an input into it’s local store, performs the processing step then stores the result into it’s local store.
- The second SPE reads the output from the first SPE’s local store and processes it and stores it in it’s output area.
This sequence can use many SPEs and SPEs can access different blocks of memory depending on the application.

If the computing power is not enough the SPEs in other Cells can also be used to form an even longer chain.

RISC like organization
- 32 bit fixed instructions
- Clean design – unified Register file

User-mode architecture
- No translation/protection within SPU
- DMA is full Power Arch protect/x-late

VMX-like SIMD dataflow
- Broad set of operations (8 / 16 / 32 Byte)
- Graphics SP-Float
- IEEE DP-Float

Unified register file
- 128 entry x 128 bit

SPU (optimized for data processing),
- Simple (FXU even)
  - Add/Compare
  - Rotate
  - Logical, Count Leading Zero
- Permute (FXU odd)
  - Permute
  - Table-lookup
- FPU (Single / Double Precision)
  - Control (SCN)
  - Dual Issue, Load/Store, ECC Handling
- Channel (SSC) – Interface to MFC
- Register File (GPR/FWD)

SMF or MFC (optimized for data transfer),
- Transfers data blocks from system memory to the local store
- Transfers data blocks from the local store to system memory
**ELEMENT INTERCONNECT BUS (C)**

- 4 X 16 byte data rings supporting multiple simultaneous transfers per ring
- 96 bytes/cycle peak bandwidth (384 Gigabytes per second)
  - However, according to IBM, 2/3 of this is likely to be achieved in practice.

**I/O AND MEMORY INTERFACES (C)**

- All the internal processing units need to be fed, so a high speed memory and I/O system is an absolute necessity.
- For this purpose Sony and Toshiba licensed the high speed “Yellowstone” and “Redwood” technologies from Rambus (a type of synchronous dynamic RAM) these are used in the XDR RAM and FlexIO.
- Both of these are interesting technologies not only for their raw speed but they have also been designed to simplify board layouts.

**PERFORMANCE COMPARISON**

<table>
<thead>
<tr>
<th>Type</th>
<th>Algorithm</th>
<th>3.2 Cell GFLOP</th>
<th>2.2 Cell GFLOP</th>
<th>Comparison Factor</th>
</tr>
</thead>
<tbody>
<tr>
<td>Basic</td>
<td>Matrix multiplication</td>
<td>21.8 GFLOP (3.2)</td>
<td>15.4 GFLOP (2.2)</td>
<td>1.4</td>
</tr>
<tr>
<td>FLOP</td>
<td>Single</td>
<td>15.4 GFLOP (2.2)</td>
<td>11.5 GFLOP (1.3)</td>
<td>1.3</td>
</tr>
<tr>
<td>FLOP</td>
<td>Double</td>
<td>31.2 GFLOP (3.2)</td>
<td>22.9 GFLOP (2.2)</td>
<td>1.3</td>
</tr>
<tr>
<td>FLOP</td>
<td>Single</td>
<td>11.5 GFLOP (1.3)</td>
<td>8.8 GFLOP (0.9)</td>
<td>1.3</td>
</tr>
<tr>
<td>FLOP</td>
<td>Double</td>
<td>22.9 GFLOP (1.3)</td>
<td>16.6 GFLOP (1.0)</td>
<td>1.3</td>
</tr>
<tr>
<td>Encryption</td>
<td>AES</td>
<td>1.1 GFLOP (0.9)</td>
<td>0.8 GFLOP (0.7)</td>
<td>1.4</td>
</tr>
<tr>
<td>Cipher</td>
<td>AES</td>
<td>0.8 GFLOP (0.7)</td>
<td>0.6 GFLOP (0.5)</td>
<td>1.4</td>
</tr>
<tr>
<td>HMAC</td>
<td>1.1 GFLOP (0.9)</td>
<td>0.8 GFLOP (0.7)</td>
<td>1.4</td>
<td></td>
</tr>
<tr>
<td>Hashing</td>
<td>SHA-512</td>
<td>0.8 GFLOP (0.7)</td>
<td>0.6 GFLOP (0.5)</td>
<td>1.4</td>
</tr>
<tr>
<td>Virtualization</td>
<td>V8 (SIMD 128-bit)</td>
<td>1.1 GFLOP (0.9)</td>
<td>0.8 GFLOP (0.7)</td>
<td>1.4</td>
</tr>
</tbody>
</table>

**I/O AND MEMORY INTERFACES (C)**

- FlexIO (communicate with peripheral devices or other CPU’s via the FlexIO Interface) and XDR RAM (MIC connects EIB to the main memory, DRAM, which is Rambus XDR that provides a bandwidth of 25.2 GB/s) both have a technology called “FlexPhase” which allows signals to come in at different times reducing the need for the wires to be exactly the same length, this will make life considerably easier for board designers working with the Cell.
- As with everything else in the Cell architecture the memory system is designed for raw speed, it will have both low latency and very high bandwidth.
SUMMARY & CONCLUSION

- Cell ushers in a new era of leading edge processors optimized for digital media and entertainment
- Desire for realism is driving a convergence between supercomputing and entertainment
- New levels of performance and power efficiency beyond what is achieved by PC processors
- Responsiveness to the human user and the network are key drivers for Cell
- Cell will enable entirely new classes of applications, even beyond those we contemplate today

THANK YOU!

CELL TEMPERATURE

<table>
<thead>
<tr>
<th></th>
<th>Sony Emotion Engine</th>
<th>Cell Processor</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU Core (x4)</td>
<td>Napa</td>
<td>64-bit Power Architecture</td>
</tr>
<tr>
<td>Core Issue Rate</td>
<td>Dual</td>
<td>Dual</td>
</tr>
<tr>
<td>Core Frequency</td>
<td>3.0GHz</td>
<td>4GHz (26%)</td>
</tr>
<tr>
<td>Core Pipeline</td>
<td>6 stages</td>
<td>21 stages</td>
</tr>
<tr>
<td>Core L1 Cache</td>
<td>16KB I-Cache + 16KB D-Cache</td>
<td>32KB I-Cache + 32KB D-Cache</td>
</tr>
<tr>
<td>Core Additional Memory</td>
<td>16KB scratch</td>
<td>512KB L2</td>
</tr>
<tr>
<td>Vector Units</td>
<td>2</td>
<td>8</td>
</tr>
<tr>
<td>Vector Registers (x, width)</td>
<td>32, 128-bit x 16, 16-bit</td>
<td>128, 128-bit</td>
</tr>
<tr>
<td>Vector Local Memory</td>
<td>4KB/16KB I-Cache + 4096/512KB D-Cache</td>
<td>256KB unified</td>
</tr>
<tr>
<td>Memory Bandwidth</td>
<td>2.3Gbps (peak)</td>
<td>25.6Gbps (peak)</td>
</tr>
<tr>
<td>Total Chip Peak FLOPS</td>
<td>6.2AFLOPS</td>
<td>296GFLOPS</td>
</tr>
<tr>
<td>Transistor Count</td>
<td>19.5 million</td>
<td>235 million</td>
</tr>
<tr>
<td>Power</td>
<td>17W @ 1.8V</td>
<td>80W (est.)</td>
</tr>
<tr>
<td>Die Size</td>
<td>240mm²</td>
<td>295mm²</td>
</tr>
<tr>
<td>Process</td>
<td>90nm, 65nm + EU</td>
<td></td>
</tr>
</tbody>
</table>