

## **CSE 533 – Advanced Computer Architectures (Spring'08)**

### **Final Project**

Due: May 27<sup>th</sup>, 2008

Run 4 integer (bzip2, gcc, mcf, vortex) and 4 FP (applu, art, mesa, mgrid) SPEC 2000 benchmarks included with the simulator. For each benchmark, skip (execute in the fast-forwarding mode) the first 50,000,000 instructions and then perform detailed cycle-accurate simulation for the following 100,000,000 instructions. Use the modified processor configuration (make it 8-way instead of 4-way) to run the benchmarks. Also, change the number of ALUs (8 Integer-ALU, 3 Mult-Div, 8 FP-adder and 3 FP Mult-Div).

Using the statistics that you have collected for the second programming assignment, implement a register cache to hold most commonly accessed registers.

#### **Latency:**

Assume 1 cycle access to the register cache, and 2-cycle access to the architectural register file. Therefore, you have to modify the original M-SIM to add an additional cycle for the register access.

#### **Size:**

Try register cache size of 4 and 8.

#### **Energy/Power:**

Use CACTI (An Integrated cache access time, cycle time, area, leakage and dynamic power model) to compute the energy requirements of the baseline model and your design. You have to collect the access statistics for the architectural register file and the register cache, separately. Then, you can integrate CACTI power numbers to estimate the energy/power dissipation of the structures.