It is possible to apply software pipelining even if there are no memory instructions inside the loop. Suggest a way to apply software pipelining to the following loops. Show the prelude and postlude sections of the code. Compare the pipeline charts of the original and software-pipelined codes. Assume the following execution latency values: ADD takes 1 cycle, MUL takes 3 cycles, DIV takes 5 cycles, STORE takes 1 cycle for execution and 1 cycle for memory stages, and, finally, BNE takes 1 cycle.

a) Loop:
   MUL R1, R2, R3
   ADDI R2, R1, #1
   STORE R2, R5, #1000
   ADDI R5, R5, #4
   BNE R5, R6, Loop

b) Loop:
   MUL R1, R2, R7
   DIV R5, R1, R3
   ADD R3, R5, R3
   ADDI R2, R2, #4
   BNE R2, R6, Loop