CSE 533: Advanced Computer Architectures
2012/2013- II

INSTRUCTOR:
Asst. Prof. Dr. Gürhan Küçük, office no. A-407, office tel. x1416, A-903, x1403
Office Hrs. Fri 10:00-11:50, 13:00-13:50 and by appointment, gkucuk@cse.yeditepe.edu.tr

CLASS SCHEDULE:
Fri 14:00-16:50, Room: A-412

TEXT:

WEB-PAGE: http://www.cse.yeditepe.edu.tr/~gkucuk/spring2013/cse533

COURSE DESCRIPTION:
Fundamentals of computer design, instruction set principles, pipelining and pipeline hazards, instruction level parallelism, overcoming pipeline hazards, superscalar, superpipelined processors, memory-hierarchy design, VLIW, CMP, SMT, MIC, Dataflow, Multicluster architectures.

TENTATIVE GRADING PLAN:
You will be given 4-6 assignments, pop quizzes, final project, a midterm and a final exam. You will give a presentation on a selected paper and write a term paper about your final project. Grade distribution is as follows:
- Paper Presentation  10%
- Assignments & Quizzes    10%
- Project & Term Paper  20%
- Midterm Exam   25%
- Final Exam   35%

• Copied assignments will be accepted as not submitted for both parties.
• Late submissions of assignments will not be accepted: if you don’t finish work on schedule, you might as well stop working on it.
• There will be a programming project. You will also be asked to write a report in a regular paper format at the end of the semester.
• You will also select and present a paper in the class at the end of the semester.

CSE 533 – Course Outline
Week 01: Introduction, Measuring and Reporting Performance, Power and Complexity
Week 02: Instruction Set Principles, MIPS ISA
Week 03: Basic Pipeline Theory, Pipeline Hazards, Handling Multicycle Operations
Week 04: Reducing and Removing Pipeline Hazards
Week 05: Dynamic Branch Prediction
Week 06: Instruction Level Parallelism, Static Instruction Scheduling
Week 07: Dynamic Instruction Scheduling
Week 08: Midterm Exam (5th of April 2013, Fri, 14:00-16:00)
Week 09: Superscalar Processors, precise interrupts in out-of-order processors, Register Renaming
Week 10: Instruction Queue, Reorder Buffer, Load/Store Queue, Architectural and Physical Register Files
Week 11: Memory Systems, Caches, SRAMs, DRAMs, virtual memory, TLBs
Week 12: Various Architectures, VLIW, EPIC, Multicluster, SMT, CMP, Many-Integrated-Core
Week 13: Paper Presentation-1
Week 14: Paper Presentation-2
Week 15: Project Demos & Term Papers