CSE425-MIDTERM

Q1. (10pts) Suppose we want to display AbCd on seven segment display of the Spartan Board. If the anode for the SSEG2 digit never gets a "0", what would we see on the display? Show your answer by coloring the leds that are turned on in the figure shown on the right side.

Q2. (20pts) Spartan board has 8 LEDs and 8 switches. Let LEDs be your outputs and switches be your inputs. Design a priority encoder using the truth table shown below. Write the Verilog code. (just use always statement)

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Q3. (5pts) Write down the equation for out of the CMOS transistor circuit shown on left hand side.

Q4. (10pts) Suppose you are given a 5-stage pipeline architecture (DLX processor) and the pipeline stages are IF=instruction fetch, ID=instruction decode, EX=execution, MEM=memory access, and WB= write back. Assume that the times required for the five functional units are as follows: 10 ns, 8ns, 10 ns, 10 ns, and 7ns. Assume pipelining adds 1ns of overhead.

a. Calculate the total time to execute 50 instructions using 5-stage pipeline architecture. Determine the clock cycle time. What are the latency and throughput?

b. Calculate the total time to execute 50 instructions on an unpipelined machine. Determine the clock cycle time. What are the latency and throughput?

Q7. (10pts) Show the results of both ALAP & ASAP scheduling of the DFG shown on the left using two multipliers (MS) and one accumulator (AF) in a schedule time of 8 cycles where:

MS : Multiplier, delay time = 2 cycles, operation = (‘*’)
AF : Fast Accumulator, delay time = 1 cycle, operations = (‘+’, ‘-’, ‘<’).
Assume MS and AF take 2 inputs.

Q8. (20pts) Draw me the state transition diagram of a pattern matcher which turns on a light when it receives a 1101 pattern (MSB comes first) and turns off the light after 3 cycles. The circuit does not have to detect more than one pattern. Write the Verilog code for your state machine.

Q9. (10pts) Come up with a scheduling (preferably the fastest) for

\[ y = ((a*b) + (c*d)) + (e*f) + (g*h) + (i*k)) \]

using only 3 multipliers and 2 adders.
Assume multiplier_delay = 2 * adder_delay.

Q10. (10pts) Design a fall-rise edge detector circuit using only NOR2 gates and a flip-flop. Then write the Verilog code for it.
Q11. (5pts) When modeling sequential logic, use nonblocking assignments. (TRUE / FALSE)

Q12. (5pts) When modeling combinational logic with an always block, use nonblocking assignments. (TRUE / FALSE)

Q13. (5pts) When modeling both sequential and combinational logic within the same always block, use nonblocking assignments. (TRUE / FALSE)

Q14. (5pts) Do not mix blocking and nonblocking assignments in the same always block. (TRUE / FALSE)

Q15. (10pts) Consider the computation $z = \left( \frac{(a+b)c*d}{e-f} \right)^{1/2}$. If the computation is to be performed repeatedly, a pipelined implementation might be contemplated. Assuming enough hardware components are available to do the computation with maximum possible parallelism, draw the flow graph by using a separate function unit for each node (multiply, divide, square-root, add, subtract) and insert registers between consecutive operations. Show the register positions on the graph. Tell me the number of pipeline stages.

Q16. (10pts) Design a circuit that multiplies an 8-bit number by 10 (in decimal) using one 8-bit adder. Write the Verilog code.

Q17. (10pts) Draw the corresponding circuit for the following code.

```verilog
module lfsrn2 (q3, clk, pre_n);
output q3;
input clk, pre_n;
reg q3, q2, q1;
always @(posedge clk)
if (!pre_n) {q3,q2,q1} <= 3'b111;
else {q3,q2,q1} <= {q2,(q1^q3),q3};
endmodule
```

GOOD LUCK 😊